

Proposal

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Independent Project
Proposal

**Design and Testing of Analogue Digital
Converters Implemented on FPGAs**

Matthew Russell

Contents

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Introduction 3

Background/ Literature Review 4

 Flash 4

 Successive-Approximation (SAR) 5

 Sigma-Delta: 5

 Pipeline 6

 Integrator – Single/Dual Slope 6

Project Design 7

Resources/ Planning..... 9

References 11

Introduction

Analogue to Digital Converters (ADCs) [1] are used extensively in embedded system as a means to convert analogue signals into a digital format which is readable by the rest of the embedded system. An example of ADCs being used is a part the signal processing stage of a radio architecture. As electronic systems have evolved so has the demand for ADCs which can compute large binary numbers at very high frequency.

The purpose of this project is to design a variety of ADCs [1] in VHDL ((Very High-Speed Integrated Circuit) Hardware Description Language) [2] using design tools such as Advanced Micro Devices (AMD) Vivado [3]. The designs will be initially tested in simulation using the Vivado environment. Once the designs are proved to be working in simulation they will be implemented onto a suitable Field Programmable Gate Array (FPGA), which is an Integrated Circuit (IC) where internal hardware can be re-configured using HDLs such as VHDL [2]. These then implemented FPGAs will be practically tested using measuring devices such as function generators and oscilloscopes to understand their performance up against industry standard parameters such as 'static performance' [4].

The underpinning aims of this project is to gather an understanding and compare the performance of the different ADC designs to establish the strengths and limitation of each design. The minimum this project will set out to achieve is to implement at least one working ADC onto a FPGA. The desired aim however, is to have at least two types where performances can be compared.

As FPGA architectures have matured, increased capability now exists to allow for a wider range of applications to be implemented in software. This project will be purely be undertaken using VHDL as a method to further develop a comprehensive understanding of the HDL. Using tools such as MatLab [5] are helpful when designing large systems to be implemented in VHDL however, the high-level abstraction means very little interaction of lower level VHDL which actually defines hardware. Therefore, using VHDL will offer the opportunity to optimise hardware aiming to show a wide-ranging competency in advanced hardware concepts such as Finite State Machines (FSM).

In terms of the specific comparison and ADC designs to discuss, the following types will be considered and a minimum of one but ideally two for comparison purposes, will be physically designed [1]:

- Flash,
- Single-Slope
- Dual-Slope,
- Successive-Approximation,
- Sigma-Delta,
- Pipeline.

Background/ Literature Review

The literature review focused on finding types of ADC's and applications already being used within industry. ADCs are used in numerous in embedded systems so finding an application was not difficult. For this project the following applications will be considered [6]:

- Embedded Control System
- Mobile Wireless telecommunications i.e. 5G.
- Defence applications such as Radar.
- Audio signals
- Medical i.e. Electroencephalogram (EEG) machines.
- Robotics
- Automotive applications i.e. Engine Control Units (ECUs)

The literature review highlighted several ADCs in use that could potentially be used:

Flash

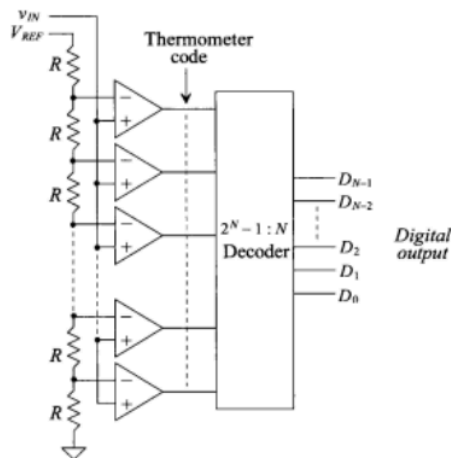


Figure 1: Flash ADC [7]

The Flash ADC is a very high speed and large bandwidth being able to output a digital value within one clock pulse. The Flash works by comparing the analogous voltage against a reference voltage using comparators. Voltages greater than the reference output a high. However, the expense of speed is size. The Flash requires $2^n - 1$ comparators and 2^n resistors where 'n' is the size in bits of the ADC. This means for higher bit applications this ADC is not viable. Further disadvantages include sparkle code and higher power consumption [1] [4].

Successive-Approximation (SAR)

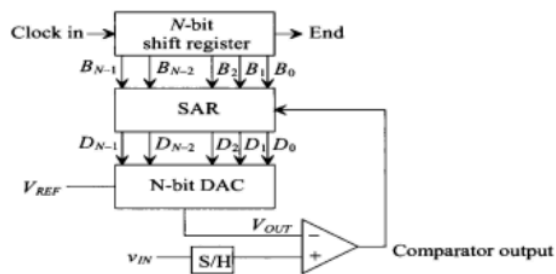


Figure 2: SAR ADC [7]

The SAR ADC is one of the most widely used ADC which can perform at low power consumption, low latency and high-speed conversion however, not as fast as the Flash. Figure 2 shows a schematic of a SAR whereby an analogous signal is compared with a DAC where each bit is compared on each clock cycle starting with the most significant bit (MSB) [1] [4].

Sigma-Delta:

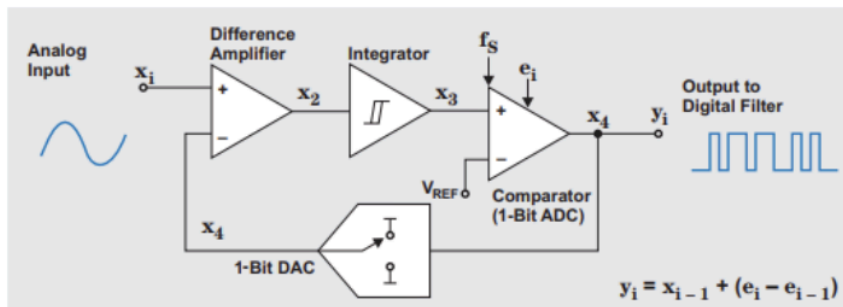


Figure 4: Sigma Delta ADC [8]

This ADC is used widely in telecommunications that use audio signals. It works by using the delta modulation [8] where the difference of between two successive samples is then quantized. This method is different from the previous ADCs whereby input signals are compared against an absolute value. The Sigma Delta is a high resolution, low noise ADC but has a high latency [1] [8].

Pipeline

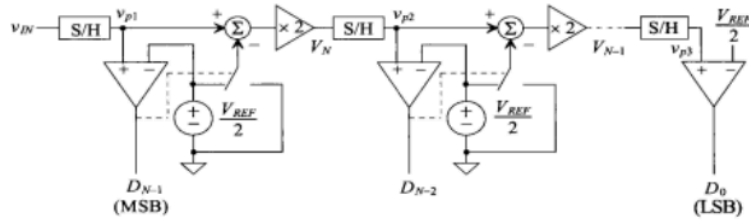


Figure 5: Pipeline ADC [7]

The Pipeline ADC is strong performer for processing high speed signals at a high resolution with a high throughput however, due to requirement that a single bit of data takes one clock cycle results in this ADC having high latency. The latency is greater than the SAR as each bit is processed by a sample and hold circuit. This therefore results in a higher power consumption requirement for the Pipeline [1] [7].

Integrator – Single/Dual Slope

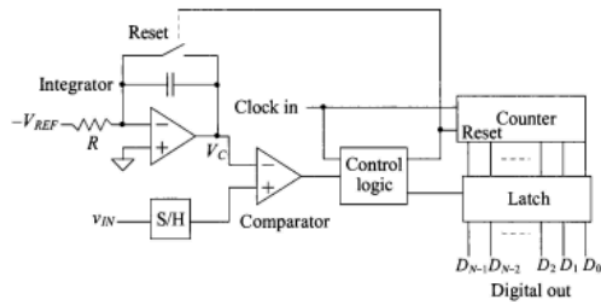


Figure 5: Integrator ADC [7]

The integrator type has high resolution but is slow and requires more power consumption compared to previous ADCs. In laymen terms the ADC works by finding how long the analogue signal takes to be integrated. This ADC comes in two forms Single and Dual slope [4] [7].

Project Design

As mentioned previously the ADCs for this project will be designed in VHDL which is a HDL for Adaptive System on Chip (SoC) devices such as FPGAs. FPGAs is a type of programmable logic containing configurable logic blocks (CLBs) and programmable interconnects that allow the user to join logic blocks to create hardware logic to perform a multitude of logic tasks. VHDL is an IEEE industry standard language for programming FPGAs [2].

Vivado [3] is a design software for FPGAs designed by AMD [3] which offers an environment to design logic from a vast library of FPGA types in HDLs such as VHDL. Vivado [3] also offers test benching in the form of synthesis, verification/simulation and implementation tools, all of which are important to ensure the FPGA is programmed properly and efficiently. The simulation tool can offer an insight to the performance of the design offering an array of reports such a timing, power as well as a schematic to see the logic blocks and Look-up-tables (LUTs) being used. Furthermore, Vivado [3] can generate bitstreams which enables the FPGA to be programmed.

Once the design is implemented onto an FPGA it will be tested practically. The IEEE standard 1241 -2010 [6] provides terminology and test methods for ADCs. However, the standard only applies to clocked ADCs (i.e. does not apply to the Flash). Nevertheless, it will provide a great resource to ensure compliance with industry standards but also use as a reference to configure a practical test setup to test the ADCs. The standard also outlines critical ADC parameters for different ADC applications which is will be a fundamental basis to determine the ADCs success. For example: a critical parameter outlined for telecommunications is bit error rate (BER) which is something that will needed to be tested for if this application is selected [6].

As well as parameters outlined in the standard the following parameters were also found from a multitude of scientific/ engineering papers [4] [6] [7] [9] [10]:

- Latency
- Power Consumption
- Bandwidth
- Precision
- DC -Static Performance
 - Input Voltage range
 - Offset Error
 - Gain error
 - Differential Non-linearity
 - Integral non-linearity
 - Total Unadjusted error (TUE)
- AC – Dynamic Performance
 - Total Harmonic Distortion (THD)
 - Signal-to-Ratio (SNR)
 - Signal-to-Noise and distortion (SINAD)

- Spurious & free dynamic range (SFDR)
- Spurious Free Dynamic Range (SFDR)
- Multi-tone Intermodulation Distortion (Multi-Tone IMD)
- Voltage Standing Wave Ratio (VSWR)
- Effective Number of Bits (ENOB)
- Clock Jitter

Unfortunately, not all these parameters will be able to be tested however, once an application is selected with aid of the IEEE Standard [6] the most important parameters appropriate to the application has be measured.

Some test equipment identified to be apart of the practical set up is included below. Like the test once an application is select so shall the best suited measuring devices [6] [9].

- Signal Generators
 - Analogue verification
 - Freq response
 - Harmonic distortion characteristics of ADCs
 - Can generate arbitrary waveforms
- Oscilloscope
 - Analogue verification
 - Digital waveform analysis
 - Trig and time measurements
- Spectrum Analysers
 - Harmonic distortion
 - Noise analysis
 - Spurious Response

Resources/ Planning

This project aims to loosely follow the FPGA programming steps outlined by MathWorks. MathWorks [5] outlines 7 steps to program FPGA:

1. Hardware Architecture Design.
2. Design.
3. Verification.
4. Synthesis.
5. Integration.
6. Implementation
7. Lab Testing and debugging

Figure 6 shows the initial time resource plan for the project. This will likely change as the project progresses and progress in some areas may be slower or quicker than predicted. The aim is to review this fortnightly and adjust timing resource plan, the ghant chart, monthly. This plan focuses on the engineering tasks and so does not include time for report writing, this however, will be done throughout the project.

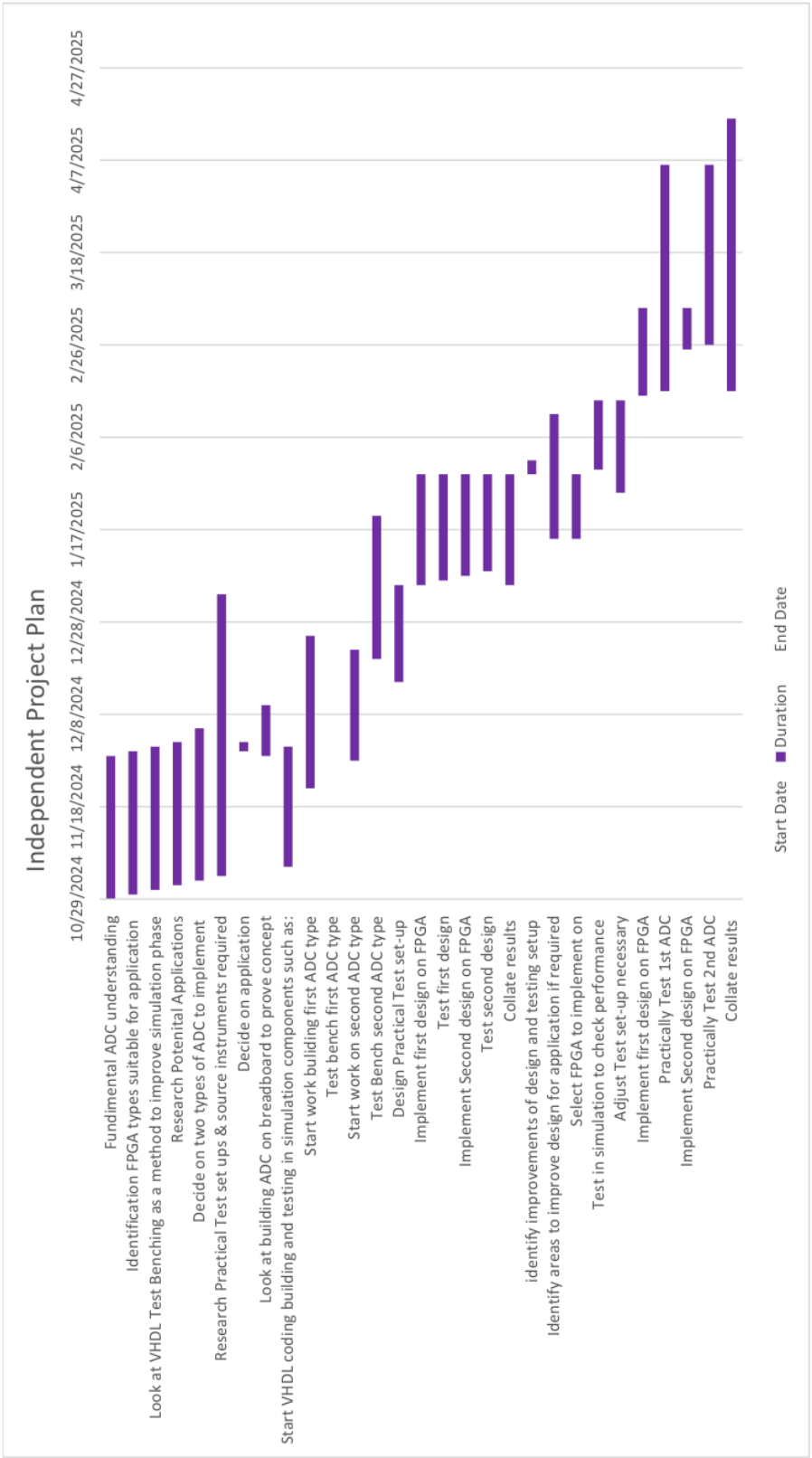


Figure 6: Gantt Chart Showing Project Time Planning outline

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Proposal

GRADEMARK REPORT

FINAL GRADE

GENERAL COMMENTS

73/100

Intro / Aims & Objectives		
The introduction clearly explains the project's aim and purpose of designing, simulating, and testing ADCs using VHDL and FPGAs, showing a well-defined approach. Including different ADC types adds depth and using tools like Vivado makes the project more practical. It is great that the text highlights the importance of ADCs in modern systems. A few small changes, like improving grammar and simplifying some phrases, could make it clearer. Well defined Aim and Purpose!	20	14
Background to the Project / Literature Review		
The inclusion of ADC types and inclusion of real time application is appreciable. The writing offers a solid comparison of their strengths and weaknesses. Adding more context about why certain ADCs are preferred in specific applications could make the review more insightful. Commendable ADC Coverage and Insights!	20	13

Project Design		
Project Design demonstrates technical knowledge but would benefit from explaining the importance of the parameters listed. For example, discussing why parameters like latency, power consumption, or THD are critical for specific applications would provide better context. Providing a brief explanation of how each parameter impacts ADC performance would strengthen the overall project design. Good Technical Knowledge!	30	23
Resources / Planning		
Thorough Resource Planning. Detailed timelines with identified tasks and durations. Completed ethics form. Good project plan!	15	12
Document Presentation		
The document is presented clearly and provides detailed explanations, showing strong planning and aligning with its purpose. The report includes thoroughness, good organization, and practical relevance. However, it could improve by avoiding repetition, improving structure, and giving clearer context for key points. Well-Outlined Content with Scope for Clarity!	15	11
TOTAL	100	73

PAGE 1
PAGE 2
PAGE 3
PAGE 4
PAGE 5
PAGE 6
PAGE 7
PAGE 8
PAGE 9
PAGE 10
PAGE 11
PAGE 12